

What is claimed is:

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5 1. A display drive circuit comprising:
RAM which sequentially stores data for image display that
is input continuously;

a plurality of grayscale pattern selection circuits, each
selecting one grayscale pattern from a plurality of grayscale
patterns, based on data stored in the RAM; and

10 a plurality of frame selection circuits which are
provided in correspondence with the plurality of grayscale
pattern selection circuits, and sequentially output grayscale
patterns selected by the plurality of grayscale pattern
selection circuits for a series of image frames.

15 2. The display drive circuit as defined in claim 1, further
comprising:

an image data conversion circuit which receives data in
which grayscales are represented by N bits (where N is an integer
greater than or equal to 2), converts the received data into
20 data in which grayscales are represented by M bits (where M is
an integer such that $M > N$), based on a set command, and supplies
the converted data to the RAM.

3. The display drive circuit as defined in claim 1, wherein
25 each of the plurality of grayscale pattern selection circuits
includes:

a selection ROM which outputs a grayscale pattern

selection signal based on data stored in the RAM; and

an FRCROM which selects one grayscale pattern from among the plurality of grayscale patterns in accordance with the outputted grayscale pattern selection signal, and uses the selected grayscale pattern to perform frame rate control (FRC) modulation in accordance with a control signal that is output from the corresponding frame selection circuit.

4. The display drive circuit as defined in claim 2, wherein each of the plurality of grayscale pattern selection circuits includes:

a selection ROM which outputs a grayscale pattern selection signal based on data stored in the RAM; and

an FRCROM which selects one grayscale pattern from among the plurality of grayscale patterns in accordance with the outputted grayscale pattern selection signal, and uses the selected grayscale pattern to perform frame rate control (FRC) modulation in accordance with a control signal that is output from the corresponding frame selection circuit.

5. The display drive circuit as defined in claim 1, wherein each of the frame selection circuits is divided into a plurality of portions that are disposed on either side of the corresponding grayscale pattern selection circuit.

6. A display drive circuit comprising:
RAM which sequentially stores data for image display that

is input continuously;

a plurality of FRCROMs which store a plurality of grayscale patterns with mutually different frame cycles, and use data stored in the RAM to select one grayscale pattern from
5 among the plurality of grayscale patterns; and

a plurality of frame selection circuits each of which sequentially outputs the selected grayscale pattern selected by the FRCROMs, for each frame,

wherein a drive signal for driving a display portion is
10 output based on the outputted grayscale pattern from the FRCROMs.

7. The display drive circuit as defined in claim 6, further comprising:

15 an image data conversion circuit which receives data in which grayscales are represented by N bits (where N is an integer greater than or equal to 2), converts the received data into data in which grayscales are represented by M bits (where M is an arbitrarily settable integer such that $M > N$), and supplies
20 the converted data to the RAM,

wherein each of the frame selection circuits outputs the selected grayscale pattern based on the M-bit grayscales, for each frame.

25 8. A semiconductor integrated circuit comprising:
the display drive circuit as defined in claim 1; and
a terminal which outputs a drive signal generated on the

14. A display panel comprising:

pixels specified by a plurality of common electrodes and
a plurality of segment electrodes, which mutually intersect;
and

5 the display drive circuit as defined in claim 1, which
drives the segment electrodes.

15. A display panel comprising:

pixels specified by a plurality of common electrodes and
10 a plurality of segment electrodes, which mutually intersect;
and

the display drive circuit as defined in claim 2, which drives the segment electrodes.

15 16. A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 3, which
20 drives the segment electrodes.

17. A display panel comprising:

pixels specified by a plurality of common electrodes and
a plurality of segment electrodes, which mutually intersect;
25 and

the display drive circuit as defined in claim 4, which drives the segment electrodes.

18. A display panel comprising:

pixels specified by a plurality of common electrodes and
a plurality of segment electrodes, which mutually intersect;

5 and

the display drive circuit as defined in claim 5, which
drives the segment electrodes.

19. A display panel comprising:

10 pixels specified by a plurality of common electrodes and
a plurality of segment electrodes, which mutually intersect;
and

the display drive circuit as defined in claim 6, which
drives the segment electrodes.

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20. A display drive method comprising:

selecting one grayscale pattern from among a plurality
of grayscale patterns having at least two types of frame cycles,
based on data for image display, and outputting the selected
20 grayscale pattern for each frame; and

outputting a drive signal for driving a display portion,
based on the selected grayscale pattern.

21. The display drive method as defined in claim 20,

25 converting grayscales of N bits (where N is an integer
greater than or equal to 2) into grayscales of M bits (where
 M is an arbitrarily settable integer such that $M > N$); and

selecting one grayscale pattern from among the plurality of grayscale patterns having at least two types of frame cycles, based on the M-bit grayscales, and outputting the selected grayscale pattern for each frame.

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